MP0107 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Eitan MEDINA et al.

Application No.: **09/348,865**

Filing Date: July 7, 1999

Group Art Unit: 2666

Examiner: Ronald Abelson

Title: A LINKING CROSS BAR CONTROLLER

MAIL STOP APPEAL BRIEF-PATENTS March 23, 2004
Commissioner for Patents
P.O. Box 1450, Alexandria, Virginia 22313-1450

Sir:

Appellants are submitting herewith, in triplicate, Appellants' Brief Under 37 CFR 1.192 in support of the Notice of Appeal filed January 23, 2004. Also enclosed is a Submission of Credit Card Payment for the $330.00 fee required by 37 CFR 1.17(c). Please charge any additional fees which may be due and owing or credit any overpayment to Deposit Account No. 08-0750.

Respectfully submitted,

HARNESS, DICKEY, & PIERCE, P.L.C.

By _____
Donald J. Daley, Reg. No. 34,313

Please address all correspondence to:

Marvell Semiconductor, Inc.
700 First Avenue, Mail Stop 509
Sunnyvale, CA 94089
Customer No. 23624
Tel. No. (408) 222-2500
Fax. No. (408) 752-9034

3/29/04 #10

MP0107

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Eitan MEDINA et al.

Application No.: **09/348,865**

Filing Date: July 7, 1999

Group Art Unit: 2666

Examiner: Ronald Abelson

Title: A LINKING CROSS BAR CONTROLLER

MAIL STOP APPEAL BRIEF-PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

March 23, 2004

APPEAL BRIEF

Sir:

In support of the Notice of Appeal filed January 23, 2004, appealing the Examiner's rejection of claims 1, 4, 5, 7, 8, 14, 15, 18, 19, 25, and 26 (and the objection of claims 9-13 and 20-24) made in the Office Action mailed November 4, 2003, Appellants submit the following arguments.

I. Real Party of Interest

The present application is assigned to Marvell Semiconductor Israel, Ltd. by an Assignment recorded on May 1, 2003 at Reel/Frame 014015/0846.

II. Related Appeals and Interferences

The undersigned, the Assignee and Appellants do not know of any appeals or interferences which would directly affect or be directly affected by or have a bearing on the Board's decision in this Appeal.

III. Status of the Claims

Claims 1, 4, 5, 7, 8, 14, 15, 18, 19, 25, and 26 stand rejected and claims 9-13 and 20-24 stand objected to by the Examiner. These are the claims on Appeal. Further, claims 2, 3, 16, 17, 27 and 28 have been allowed and are not on Appeal. Claims 6 has been cancelled during prosecution. Each of the pending claims are reproduced in the attached Appendix A.

IV. Status of the Amendments

No Amendments or Replies have been filed under 37 C.F.R. 1.116.

V. Summary of the Invention

The present application, in one embodiment, is directed to a data network including at least one crossbar 10 of Figs. 2-4, which includes N ports 10 of Figs. 1-4. Crossbar 10 includes a plurality of devices such as a plurality of switches 12 of Figs. 1-4. Each of the switches 12 is associated with and connected to one port 16 of Figs. 1-4 of the crossbar 16 (see page 6, line 1-page 7, line 2).

As shown in Figs. 2-4, in an exemplary embodiment, the N ports 16 equal four (4) in number, as do the N switches 12 (four (4) switches 12, each associated with and connected to one of four (4) ports 16). This is significant because each one port 16 of the crossbar 10 comprises N-1 output buffers (three (3) in Figs. 2-4), each corresponding to an another one of the remaining other N-1 ports (see page 7, lines 3-24).

One exemplary embodiment of this is shown in Figure 2 of the present application, which includes N ports numbered 16 (for example, four (4) ports as shown in the example of Figure 2),

with each port including N-1 output buffers 22 (in the example of Figure 2, three (3) output buffers). Each of the N-1 (three in this example) output buffers correspond to one of the other (three in this example) ports (in the example shown in Figure 2, the port 16 corresponding to switch A includes three output buffers, one corresponding to each of ports B, C, and D; the port 16 corresponding to switch D includes three output buffers corresponding to each of ports C, B, and A; etc.). As such, each crossbar includes a number of ports, with each port including a number of output buffers which is one less than the total number of ports (three output buffers and four ports as shown in the example of Figure 2), each output buffer corresponding to one of the other ports. As such, each of the plurality of N-1 of port output buffers receives messages only from a corresponding input buffer of one of the N-1 other ports.

Based upon such a configuration, data packet flow between ports of the crossbar can be executed efficiently. Port to port communication is achieved via point to point connection between input buffers 20 and their associated output buffers 22. For example, input buffer 20A of port 16A transfers data to output buffers 22 located at ports 16B, 16C, and 16D (see page 7, line 23-page 8, line 21). Each port 16 is linked to a corresponding switch 12. As such, each port can receive data from any one of the three other ports and thus, even if one port is busy, traffic to another port can continue in an efficient manner (see page 9, line 4-page 10, line 17). Hence, in contrast to prior network systems which required a total data flow halt upon collision from data backups, the control flow of the configuration of the present system allows data flow to continue (see page 12, lines 10-13).

Note that the aforementioned Summary of the Invention, including indications of reference numerals, drawing figures, and paragraphs and page numbers of the application which have been provided solely to comply with U.S. Patent and Trademark Office rules concerning the appeal of claims of an application. The above-mentioned descriptions are merely exemplary and should not be considered, in any way, to limit the claims of the present application.

VI. Issues

i. Whether or not claims 7, 8, 14, 19, and 25 are unobvious under 35 U.S.C. § 103(a) over the teachings of Daines et al. (U.S.P. 6,192,422) in view of Calvignac et al. (U.S.P. 6,370,148), and whether or not the reference combination is proper; and

ii. Whether or not claims 1, 4, 5, 15 and 16 are unobvious under 35 U.S.C. § 103(a) over the teachings of Daines et al. (U.S.P. 6,192,422) in view of Calvignac et al. (U.S.P. 6,370,148) and further in view of Ogimoto et al. (U.S.P. 6,032,205), and whether or not the reference combination is proper.

VII. Grouping of Claims

Appellants respectfully request, for the purposes of this Appeal, that the grouping of the claims be as follows:

Group (i) including claims 9-13 and 20-24;

Group (ii) including claims 7 and 18;

Group (iii) including claims 8 and 19;

Group (iv) including claims 14 and 25;

Group (v) including claim 1;

Group (vi) including claim 4;

Group (vii) including claims 5/1 and 5/4; and

Group (viii) including claims 15 and 26.

VIII. Arguments

A. Group (i) including allowable subject matter of claims 9-13 and 20-24

Initially, Appellants note that the Examiner has indicated that claims 2, 3, 16, 17, 27, and 28 are allowed in connection with the present application. Based on the Examiner's indication, each of independent claims 2, 16, 17, 27, and 28 (and dependent claim 3) have been allowed. Further, claim 5 as dependent upon allowable claims 2 and 3 (5/2, and 5/3) is also allowable. These claims are not the subject of this Appeal.

Further, the Examiner has admitted that claims 9-13 and 20-24 contain allowable subject matter and would be allowable if rewritten in independent form. Accordingly, irrespective of the outcome of this Appeal, Appellants reserve the right to re-write any and all of these objectionable claims into independent form to place them in condition for allowance.

B. Group (ii) including claims 7 and 18

1. Prior Art Rejection

The Examiner has rejected claims 7 and 18 under 35 U.S.C. § 103 (a) as being unpatentable over Daines et al. (U.S. Patent No. 6,192,422) in view of Calvignac et al. (U.S. Patent No. 6,370,148).

Regarding claims 7 and 18, the Examiner alleges that Daines et al. teaches a method and apparatus for a crossbar (Figure 2) communicating with at least one device (citing Figure 2, node 14, and column 4, lines 41-44). The Examiner alleges that each crossbar comprises N ports (citing Figure 2; port A...N). The Examiner further alleges that each port comprises a link logic unit to receive messages and date from a respective device (citing Figure 2, box 18 and column 4, lines 53-55). The Examiner further alleges that each port comprises an input buffer to restore data from the respective device (citing Figure 2, box 20). The Examiner additionally alleges that each port comprises a port arbiter to select one of the N-1 ports to output data to (citing Figure 2, boxes 25 and 26, and column 5, lines 25-40). Finally, the Examiner alleges that each input buffer transfers the stored data to one of the other said N ports (citing Figure 2, box 20 and column 5, lines 6-15).

Regarding the Daines et al. patent, the Examiner admits that Daines et al. fails to teach N-1 output buffers, each corresponding to N-1 ports.

The Examiner alleges that Calvignac et al. teaches N-1 buffers (Figure 1, box 120 A...D) corresponding to N-1 ports (Figure 1 A...D) and an arbitrator (Figure 1, box 110).

In attempting to combine the referenced teachings, the Examiner alleges that it would have been obvious to one of ordinary skill in the art, having both Daines et al. and Calvignac et al. before him/her and with the teachings [A] as shown by Daines et al., a crossbar communicating with at least one device, and [B] as shown by Calvignac et al., N-1 buffers corresponding to N-1 ports and an arbitrator, to be motivated to modify the system of Daines et al. by replacing a single output buffer (Figure 2, box 24) and a centralized arbiter (Figure 2, box 26) with N-1 output buffers and an arbiter for each port. The Examiner alleges that this would improve the system by allowing for more than one input buffer to communicate over the bus at a time. The Examiner admits that at present, only one input buffer communicates over the bus at a time (see Daines et al., column 5, lines 30-40). The Examiner further states that as seen above,

the Examiner corresponds applicant's crossbar (Figure 2, box 10M) with the repeater (Figure 2, box 10) of Daines et al. The Examiner states that as seen by Newton, a crossbar is simply a means for transferring inputs to outputs.

2. Arguments Traversing the Examiner's Rejection of claims 7 and 18

Independent claim 7 is directed to a crossbar comprising N ports. **Each port includes a N-1 output buffers**, each corresponding to another one of said N-1 other ports.

Thus, for example, as shown in Figure 2 of the present application (which supports the claims of the present application, but to which the claims of the present application are not necessarily limited), the crossbar 10 includes four switches A, B, C, D associated with and connected to one of the four ports 16 of the crossbar, with each port 16 including an input buffer and three output buffers. **Thus, in the example of Fig. 2, there are 4 ports, each with three output buffers.** With regard to switch A as shown in Figure 2 for example, the port 16 of switch A includes a single input buffer 20A for sending messages to the other N-1 ports of the crossbar (the other three ports of the crossbar, namely port B, port C, and port D); and N-1 or three (3) output buffers 22B, 22C, and 22D, **each corresponding to one of the other N-1 (the other three) (3)) ports of the device.** As such, efficient communication and data flow is possible.

As admitted by the Examiner, Daines et al. fails to teach or suggest N-1 output buffers each corresponding to N-1 ports. More specifically, with regard to claim 7, Daines et al. fails to teach or suggest a crossbar including N ports, with each one port of the crossbar comprising N-1 output buffers, each corresponding to **another one** of said N-1 ports. To the contrary, Daines et al. is directed to a repeater including a plurality of ports, with each of the ports including **an input buffer and an output buffer**. In other words, a single output buffer at a port stores data from **each of the input buffers of the other ports.** As such, Daines et al. is merely an example of a conventional device, and suffers the same drawbacks enumerated above.

In an attempt to make up for the deficiency of Daines et al., the Examiner attempts to combine its teachings with those of Calvignac et al. Appellants respectfully submit that even assuming or going under the Calvignac et al. could be combined with Daines et al., which Appellants do not admit, Calvignac et al. would still fail to make up for at least the aforementioned deficiency of Daines et al.; and further submit that the Examiner has not

provided proper motivation regarding why one of ordinary skill in the art would be led to combine the teachings of Calvignac et al. with those of Daines et al.

Initially, Appellants respectfully submit that the Examiner has not even properly characterized the deficiency of Daines et al. The Examiner admits that Daines et al. fails to teach N-1 output buffers, each corresponding to N-1 ports. While this is true, claim 7 actually refers to N ports, wherein each one port includes a N-1 output buffers, each corresponding to anther one of said N-1 ports. **Thus, Daines et. al. actually fails to teach or suggest N-1 output buffers for each of N ports.**

Throughout the prosecution of the present application, which has included four non-final Office Actions and two personal interviews, the Examiner has failed to find any reference which makes up for the aforementioned deficiency of Daines et al. In each of the various patents applied throughout the prosecution of the present application, **they always include an equal number of input and output ports** (never N-1 output buffers for each of N ports, with each of the N-1 output buffers corresponding to another one of the N-1 ports as claimed in claim 7).

With regard to the newly applied **Calvignac et al. reference, this reference similarly includes an equal number of output buffers to ports.** As discussed in the paragraph bridging columns 3 and 4 of the patent, Figure 1 shows a packet switch having **four inputs** denoted a, b, c, and d and **four outputs** A, B, C, and D. There is never any mention of N-1 output buffers for each of the N ports, as is claimed in claim 7 of the present application. Accordingly, even assuming *arguendo* that Calvignac et. al. could be combined with Daines et. al., which Appellants do not admit, the alleged combination would still fail to teach or suggest the aforementioned limitation of claim 7. Accordingly, the rejection must be reversed.

The Examiner alleges that Calvignac et al. teaches N-1 buffers, as shown in Figure 1, box 120, citing elements a, b, c, and d. He further alleges that this corresponds to N-1 ports, citing Figure 1A, B, C, and D. Even if this is the case, the Examiner is confused as such a recitation of **Calvignac et al. does not meet at least the limitation set forth in claim 7 of the present application, which includes N ports (not N-1 ports as indicated by the Examiner in this rejection), and N-1 output buffers.** Whether the Examiner states that Calvignac et al. teaches N-1 output buffers correspond to N-1 ports, or N output buffers corresponding to N ports, it is still an **equal number of output buffers, equal in number to the number of ports**. This is clearly different from the present invention set forth in claim 7 and thus, even assuming

arguendo that Calvignac et al. could be combined with Daines et al., which Appellants do not admit, the alleged combination would still fail to meet at least the aforementioned limitation of claim 7 of the present application.

Although claim 7 of the present application is supported by, but not limited to the embodiment shown in Figure 2, the embodiment shown in Figure 2 does illustrate the distinction between the system of both Daines et al. and Calvignac et al., taken either singly or in combination. As shown in Figure 2, the crossbar includes N ports, namely four ports 16 corresponding to switches A, B, C, and D. Each of the four ports 16 includes an input buffer and three (N-1) output buffers, each corresponding to one of the other ports. The port 16 corresponding to switch A, for example, includes an input buffer A and three output buffers 22 labeled so as to correspond to ports B, C, and D, respectively. Again, although this is merely exemplary of that shown in claim 7, it clearly illustrates how claim 7 is supported by Figure 2 of the present application, and how the aforementioned limitations of claim 7, including a crossbar comprising N ports, with each port including N-1 output buffers, distinguishes from the teachings of Daines et al. and Calvignac et al., taken either singly or in combination.

Still further, even assuming *arguendo* that the teachings of Calvignac et al. could makeup for the deficiencies of Daines et al., which Appellants do not admit for at least the aforementioned reasons, **the Examiner has still failed to meet his burden of providing proper motivation for combining the teachings of Calvignac et al. with that of Daines et al.** as required by the Court of Appeals for the Federal Circuit (CAFC), to establish obviousness based on a combination of elements disclosed in the prior art, there must be some motivation, suggestion, or teaching of the desirability of making the specific combination that was made by the Appellants (some "instructions" for putting pieces together, not just the pieces). The motivation, suggestion, or teaching may come explicitly from statements in the prior art, from the knowledge of one ordinary skill in the art, or in some cases, from the nature of the problem to be solved. See *In re Dembiczak,* 50 USPQ 1614 (Fed. Cir. 1999).

The Examiner has recognized a deficiency in Daines et al., and has merely attempted to find the missing piece of this puzzle, without finding the necessary "instructions" for putting the piece together with the remainder of the puzzle. **In other words, the Examiner has not found or provided any indication as to why the two pieces of prior art should be combined**, which is required to establish *prima facie* case of obviousness under 35 U.S.C. § 103. See *Dembiczak,*

50 USPQ 2d at 1617. Broad conclusary statements standing alone, as provided by the Examiner, are not "evidence". The Examiner has merely utilized Appellants' invention, in hindsight, to provide the teaching or suggestion for combining the references. This is clearly an improper use of hindsight.

In the present situation, the Examiner merely alleges that it would have been obvious to modify the system of Daines et al. by replacing its admitted single output buffer (Figure 2, box 24), and a centralized arbiter (Figure 2, box 26), with N-1 output buffers and an arbiter for each port, based on the alleged teachings of N-1 buffers corresponding to N-1 ports and an arbitrator as allegedly taught by Calvignac et al. (noting that the teachings of N-1 buffers and N-1 ports still does not satisfy the limitations set forth in claim 1). The Examiner alleges that this modification of Daines et al. in view of Calvignac et al. would improve the system by allowing for more than one input buffer to communicate over the bus at a time, admitting that only one input buffer communicates over the bus at a time, as taught by column 5, lines 30-40 of Daines et al. Regarding this alleged motivation, however, the Examiner has provided **no evidence** of this motivation as required to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 as set forth above. Further, Appellants do not understand how including N-1 output buffers corresponding to N-1 ports has anything to do with permitting input buffer communication as alleged by the Examiner. Even if the aforementioned motivation were true, which Appellants do not admit, the motivation would merely lead one of ordinary skill in the art to vary the number of input buffers and/or connections, and not to vary the number of output buffers. Accordingly, the Examiner's rejection cannot stand and must be overturned.

Finally, the Examiner states that "As seen above, the Examiner corresponds the Applicants' crossbar (Figure 2, box 10m) with the repeater (Figure 2, box 10) of Daines et al. As seen by Newton, ... a crossbar is simply a means for transferring inputs to outputs." Appellants do not understand this quote made by the Examiner at the bottom of page 3 of the Office Action of November 4, 2003. Appellants further note that the reference to "Newton" is irrelevant as Newton is not part of the Examiner's rejection. Finally, Appellants do not see any relevance in this quote made by the Examiner.

With regard to claim 18, although claim 18 should be governed only by the limitations present therein, claim 18 is allowable for at least reasons somewhat similar to some of those set forth with regard to claim 7 above. Claim 18 is directed to a crossbar including N port means,

wherein each one of the N port means comprises at least N-1 buffer means. At least such a teaching of a crossbar including an unequal number of N port means and N-1 output buffer means, is not taught or suggested by Daines et al. or Calvignac et al., taken either singly or in combination. Further, for the reasons set forth above with regard to claim 7, the Examiner has failed to establish a proper *prima facie* case of obviousness under 35 U.S.C. § 103 and has provided **no evidence** of motivation to combine the teachings of Daines et al. and Calvignac et al, as required to establish a *prima facie* case of obviousness under 35 U.S.C. § 103. Accordingly, the Examiner's rejection of claim 18 must be overturned.

C. Group (iii) including claims 8 and 19

1. Rejection of claims 8 and 19

The Examiner has rejected claims 8 and 19 under 35 U.S.C.§103 as being unpatentable under Daines et al. in view of Calvignac et al. Regarding claims 8 and 19, the Examiner alleges that the logic link unit determines a type of message from a respective device as taught by column 4, lines 60-62 (noting that the Examiner does not indicate whether these column and lines relate to Daines et al., Calvignac et al., or any other reference). The Examiner alleges that in order for the MAC to convert the digital data to an Ethernet frame, the MAC must know what type of data exists. Again, the Examiner provides no support for this rejection.

2. Arguments Traversing the Examiner's Rejection of claims 8 and 19

Regarding claims 8 and 19, Appellants respectfully submit that these claims are allowable for at least the reasons previously presented with regard to their respective corresponding independent claims 7 and 18.

Further, with regard to the logic link unit as set forth in claim 8 and/or the logic link means as set forth in claim 19, each of which determines a type of message from the respective device, neither of these limitations is met by the teachings of Daines et al. or Calvignac et al., taken either singly or in combination. Column 4, lines 60-62 of Daines et al. refers to a MAC inverting the stream of digital signals. There is no indication that this MAC determines a type of message from a respective device as set forth in claims 9 and 18. Similarly, in Calvignac et al., column 4, lines 60-62 also fails to teach or suggest any type of determining of a type of message

from a respective device as set forth in claims 8 and 19, wherein Calvignac et al. merely refers a matrix element in input and output routing.

Further, for the reasons set forth above with regard to claim 7, the Examiner has failed to establish a proper *prima facie* case of obviousness under 35 U.S.C. § 103 and has provided **no evidence** of motivation to combine the teachings of Daines et al. and Calvignac et al, as required to establish a *prima facie* case of obviousness under 35 U.S.C. § 103. Accordingly, the rejection must be overturned.

D. Group (iv) including claims 14 and 25

1. Prior Art Rejection

Regarding claims 14 and 25, the Examiner rejects these claims under 35 U.S.C. § 103 as being unpatentable over Daines et al. in view of Calvignac et al. Specifically, the Examiner admits that although Daines et al. is silent on the issue of the device being unable to receive data, and the device providing a message to a link logic unit or means, the Examiner alleges that the inventor teaches the inhibiting signal in the reverse direction (citing column 7, lines 5-13). The Examiner then alleges that **it would be logical** to have inhibiting signals traveling in both directions. He alleges "Just as in port input buffer is monitored, the node's buffer **could be** monitored for an overflow condition." He states that if this condition is met, the device **could send** an inhibit signal to the port. The Examiner alleges that then the logic link means (Figure 2, box 18) would inform the arbiter (Figure 2, box 25) to inhibit communication. The Examiner finally alleges this would improve the system by preventing the device (Figure 2, box 14) from overflowing.

2. Arguments Traversing the Examiner's Rejection of claims 14 and 25

With regard to claims 14 and 25, these claims are initially allowable for at least the reasons previously set forth regarding their corresponding independent claims.

In addition, as admitted by the Examiner, neither Daines et al. nor Calvignac et al., taken either singly or in combination, teach or suggest the limitations set forth in claims 14 and 25,

directed to a device providing a message to a link logic means or unit if the device is unable to receive data, and indicating that the link logic means or unit signals an arbiter means or arbiter to inhibit communication to the device.

The Examiner merely alleges that in his mind, it would be logical to have inhibiting signals traveling in both directions; that a node buffer's condition **could be** monitored for an overflow condition; and the device **could send** an inhibit signal to the port if a condition is met. The Examiner's opinion, and what would be logical, what could be monitored, and what could be sent, **are not the proper test for determining obviousness under 35 U.S.C. § 103**. As set forth *In re Dembiczak* above and as further set forth in *In re Sang Lee*, 61 USPQ2d 1430 (Fed.Cir. 2002), stating what could be or might be is not "**evidence**" of any teaching or suggestion for one of ordinary skill in the art to modify the teachings of one or both of the references. Relying on the Examiner's opinion or common knowledge or common sense, without any specific hint or suggestion of this in a particular reference, is not the standard for reaching the conclusion of obviousness. See *In re Sang Lee, supra.* If the Examiner is relying on personal knowledge to support a finding of what is known in the art, the Examiner **must provide** an affidavit or declaration setting forth specific factual statements and explanations to support the finding. See 37 C.F.R. §1.104(d) and MPEP 2144.03(c).

Further, for the reasons set forth above with regard to claim 7, the Examiner has failed to establish a proper *prima facie* case of obviousness under 35 U.S.C. § 103 and has provided **no evidence** of motivation to combine the teachings of Daines et al. and Calvignac et al, as required to establish a *prima facie* case of obviousness under 35 U.S.C. § 103.

Accordingly, Appellants respectfully challenge the Examiner's use of personal opinion and note that as an affidavit or declaration has not been provided, the rejection must be overturned.

E. Group (v) including claim 1

1. Rejection

The Examiner has rejected claim 1 under 35 U.S.C. §103 as being unpatentable over Daines et al. in view of Calvignac et al., and further in view of Ogimoto et al..

Specifically, regarding claim 1, the Examiner alleges that the combination of Daines et al. and Calvignac et al. teaches all the elements of claim 1 except for a plurality of N-1 fullness sensors, each associated with one output port buffer, for measuring the fullness state of its associated port output buffer, and a shut-off means, indicating to the device connected to the one port not to send data for the port.

The Examiner alleges that Ogimoto et al. teaches a plurality of N-1 fullness sensors, each associated with one port output buffer, for measuring the fullness state of its associated port output buffer (citing Figure 1, box 122-125, and column 13, lines 43-49); and a shut-off means, indicating to the device connected to said one port not to send data for the port (citing column 13, lines 43-49). The Examiner further alleges that it would have been obvious to one of ordinary skill in the art to combine such teachings of Ogimoto et al. with the alleged combination of Daines et al. and Calvignac et al. because one of ordinary skill in the art would arguably be motivated to modify the system of the combination of Daines et al. and Calvignac et al. by connecting the output monitoring circuit of Ogimoto et al. to each of the output buffers of Daines et al. The Examiner alleges that this would improve the system by preventing overflow in the output buffers.

2. Arguments Traversing the Examiner's Rejection of claim 1

Claim 1 requires a crossbar comprising N ports, with each one port comprising an input buffer and a plurality N-1 of port output buffers, each corresponding to one of said N-1 other ports. Thus, for reasons somewhat similar to those presented above regarding independent claim 7, Appellants respectfully submit that claim 1 is allowable over the alleged combination of Daines et al. and Calvignac et al., even assuming *arguendo* that they could be combined. Further, even assuming *arguendo* that Ogimoto et al. could be combined with Daines et al. and Calvignac et al., which Appellants do not admit, Ogimoto et al. would also fail to make up for at least the aforementioned deficiencies of Daines et al. and Calvignac et al.

As admitted by the Examiner during the prosecution of the application, and as especially discussed in the personal interview of April 1, 2003, Ogimoto et al. fails to teach or suggest the limitation of a plurality of N-1 port output buffers, as well as the limitation of each of the "plurality of N-1 port output buffers receives said messages only from a corresponding input

buffer corresponding to one of said N-1 other ports", as set forth in claim 1 of the present application. Ogimoto et al., somewhat similar to Daines et al. and Calvignac et al., **teaches only one input buffer and one output buffer corresponding to each node**, wherein an output buffer is capable of receiving messages from **any one** of the input buffers. Thus, Ogimoto et. al. similarly fails to teach or suggest N ports with N-1 output buffers. Accordingly, for at least the reasons previously set forth regarding claim 7 above, and for at least these additional reasons, Appellants respectfully submit that claim 1 is allowable over the alleged combination of Daines et al., Calvignac et al. and Ogimoto et al.

Further, for the reasons set forth above with regard to claim 7, the Examiner has failed to establish a proper *prima facie* case of obviousness under 35 U.S.C. § 103 and has provided **no evidence** of motivation to combine the teachings of Daines et al. and Calvignac et al, as required to establish a *prima facie* case of obviousness under 35 U.S.C. § 103.

Still further, somewhat similar to that set forth above, the Examiner has shown no evidence as to why one of ordinary skill in the art would be led to combine the teachings of Ogimoto et al. with either one or both of Daines et al. and Calvignac et al. The Examiner has merely alleged in his opinion, that connecting output buffer monitoring circuits of Ogimoto et al. to the output buffers of Daines et al. would improve the system by preventing overflow in the output buffers. However, even if this were true, and even if this combination could be made, this is still not evidence of motivation as required by the Court of Appeals for the Federal Circuit. Without such evidence, the alleged combination cannot be made. Accordingly, the rejection must be overturned.

Finally, as admitted by the Examiner during the prosecution of the application, Ogimoto et al. fails to teach or suggest the limitation of each of the "plurality of N-1 port output buffers receives said messages only from a corresponding input buffer corresponding to one of said N-1 other ports", as set forth in claim 1 of the present application. As indicated above, Ogimoto et. al., somewhat similar to each of Daines et al. and Calvignac et al, teaches only one input buffer and one output buffer corresponding to each node, wherein an output buffer is capable of receiving messages from **any one** of the input buffers. As such, an output buffer cannot receive messages **ONLY** from a corresponding input buffer as claimed in claim 1. Accordingly, as this additional limitation is also not taught or suggested by any of Ogimoto et. al., Daines et al. and

Calvignac et al, taken either singly or in combination, claim 1 is allowable and the rejection must be overturned.

F. Group (vi) including claim 4

1. Rejection

The Examiner has rejected claim 4 under 35 U.S.C. §103 as being unpatentable over Daines et al. in view of Calvignac et al. and in view of Ogimoto et al. With regard to claim 4, the Examiner alleges that a port arbiter to control the transmission of data to the respective device is present in Daines et al., citing Figure 2, box 25 and column 5, lines 25-27. The Examiner alleges that it is obvious not to send data to a device that is full and alleges that if the device is full, it cannot process more information.

2. Arguments Traversing the Examiner's Rejection of claim 4

Initially, Appellants respectfully submit that dependent claim 4 is allowable over the alleged combination of references for at least the reasons previously presented regarding corresponding claim 1.

Further, as essentially admitted by the Examiner, neither Daines et al., nor any of the other references, teaches or suggests each crossbar comprising an arbiter for providing messages from the N-1 output buffers to the device connected to its port only if the device is not full, as claimed in claim 4. None of the references teach or suggest N-1 port output buffers, let alone an arbiter which performs the stated functions.

Further, for the reasons set forth above with regard to claims 1 and 7, the Examiner has failed to establish a proper *prima facie* case of obviousness under 35 U.S.C. § 103 and has provided **no evidence** of motivation to combine the teachings of Daines et al., Calvignac et al and/or Ogimoto et al., as required to establish a *prima facie* case of obviousness under 35 U.S.C. § 103. Accordingly, the rejection must be overturned.

G. Group (vii) including claims 5/1 and 5/4

1. Rejection

The Examiner has rejected claim 5 under 35 U.S.C. §103 as being unpatentable over Daines et al. in view of Calvignac et al. and further in view of Ogimoto et al. Regarding claims 5/1 and 5/4, the Examiner alleges that Daines et al., in Figure 2, element 16, indicates each port comprising a bus link connected to the device.

2. Arguments Traversing the Examiner's Rejection of claims 5/1 and 5/4

Appellants initially note that claim 5 depends from each of claims 1-4. As claims 2 and 3 stand allowed in connection with the present application, claims 5/2 and 5/3, as dependent upon claims 2 and 3, are also allowable. Thus, the present Appeal deals only with claim 5 as dependent upon claim 1, and claim 5 is dependent upon claim 4.

Further, Appellants respectfully submit that claims 5/1 and 5/4 are allowable for at least the reasons previously presented regarding corresponding claim 1, upon which claims 5/1 and 5/4 are dependent. For the reasons set forth above with regard to claims 1 and 7, the Examiner has failed to establish a proper *prima facie* case of obviousness under 35 U.S.C. § 103 and has provided **no evidence** of motivation to combine the teachings of Daines et al., Calvignac et al and/or Ogimoto et al., as required to establish a *prima facie* case of obviousness under 35 U.S.C. § 103. Accordingly, regarding claim 5 as dependent upon claim 1, and claim 5 as dependent upon claim 4, these aspects of claim 5 are allowable for at least the reasons previously submitted regarding independent claim 1 of the present application. Accordingly, the rejection must be overturned.

H. Group (viii) including claim 15 and 26

1. Rejection

The Examiner has rejected claims 15 and 26 under 35 U.S.C. §103 as being unpatentable over the combination of Daines et al. and Calvignac et al. as applied to claims 7 and 18 above, and further in view of Ogimoto et al. The Examiner admits that the combination of Daines et al. and Calvignac et al. is silent on if an n^{th} one of the N-1 output buffers is at least a predetermined

capacity, a signal is sent to the n^{th} one of the port arbiter of the other of N-1 ports to inhibit further transmission. The Examiner alleges that Ogimoto et al. teaches a plurality of N-1 fullness sensors, each associated with one port output buffer, for measuring the fullness state of its associated port output buffer (citing Figure 1, box 122-125, and column 13, lines 43-49); and a shut-off means, indicating to said device connected to the said one port not to send data for the port (column 13, lines 43-49). The Examiner then alleges that it would be obvious to one of ordinary skill in the art to modify the system of the combination of Daines et al. and Calvignac et al. by connecting the output buffer monitoring circuit of Ogimoto et al. to reach the output buffers of Daines et al. The Examiner alleges that this would improve the system by preventing overflow in the output buffers.

2. Arguments Traversing the Examiner's Rejection of claims 15 and 26

Initially, regarding claims 15 and 26, Appellants respectfully submit that even assuming *arguendo* that Ogimoto et al. could be combined with one or both of Calvignac et al. (which Appellants do not admit), Ogimoto et al. would still fail to make up for at least the previously mentioned deficiencies of independent claims 7 and 18 for the reasons set forth above. Thus, claim 15 and 26 are allowable for at least the reasons set forth above regarding claims 7 and 18. Accordingly, the rejection should be overturned.

Further, with regard to claims 15 and 26, as **none of the references teach or suggest the inclusion of N-1 output buffers** as included in claims 15 and 26, none of the references can provide teaching or suggestion of the complete limitations set forth in claims 15 and 26. Accordingly, for at least these additional reasons, even assuming *arguendo* that Ogimoto et al. could be combined with either one or both of Daines et al. and Calvignac et al., which Appellants do not admit for the reasons expressed above regarding the rejection of claim 1, the alleged combination would still fail to render any of claims 15 and 26 obvious. In addition, for the reasons previously set forth, it would not be obvious to one of ordinary skill in the art to combine the teachings of Ogimoto et al. with those of Daines et al. and Calvignac et al.; and the Examiner has provided no such evidence of why one of ordinary skill in the art would be led to make any such reference combination. Accordingly, for at least these additional reasons, Appellants respectfully submit that claims 15 and 26 are allowable over the prior art.

Further, for the reasons set forth above with regard to claims 1 and 7, the Examiner has failed to establish a proper *prima facie* case of obviousness under 35 U.S.C. § 103 and has provided **no evidence** of motivation to combine the teachings of Daines et al., Calvignac et al and/or Ogimoto et al., as required to establish a *prima facie* case of obviousness under 35 U.S.C. § 103. Accordingly, the rejection must be overturned.

IX. CONCLUSION

In summation, Appellants note that:

1) The Examiner has failed to meet his burden of creating a *prima facie* case of obviousness.

2) The Examiner has clearly ignored limitations present in the independent claims, wherein limitations generally stated as "N ports with N-1 output buffers" are clearly are not taught or suggested by either of the prior art references to Daines et al. or Calvignac et al.

3) Further, the Daines et al. and Calvignac et al. systems are two completely different systems which would not lead anyone of ordinary skill in the art to combine their teachings or suggestions in that one deals with the problems of a processor pipeline, and the other deals with the problems of transmitting data packets between nodes of a local area network.

4) The prior art reference to Calvignac et al. does not makeup for the admitted deficiencies of Daines et al., and further includes teachings which are not in anyway taught or suggested to be combined with the teachings of Daines et al. Similarly, the prior art to Ogimoto et. al. does not makeup for the admitted deficiencies of Daines et al. and Calvignac et al., and further includes teachings which are not in anyway taught or suggested to be combined with the teachings of Daines et al and Calvignac et al..

5) Even assuming *arguendo* that there might be some reason to try some of the aspects of Calvignac et al. in a system such of that of Daines et al., or to try some aspects of Ogimoto et. al. in the system of Daines et al. and Calvignac et al, that is still not the proper standard for determining obviousness. There must be more than some possibility of trying certain teachings; there must be some reason, suggestion, or motivation provided somewhere, which would lead one of ordinary skill in the art to modify the teachings of one reference to include the teachings of another. No such reason, suggestion, or motivation has been provided

by the Examiner. Accordingly, for at least such reasons, Appellants respectfully submit that all outstanding prior art rejections must be overturned and that each of independent claims 1, 7, and 18, and all claims dependent thereon, must be passed to allowance.

The Examiner has already allowed claims 2, 3, 5/2, 5/3, 16, 17, 27 and 28 in connection with the present application. Further, the Examiner has objected to claims 9-13 and 20-24 in connection with the present application, indicating that they contain allowable subject matter. With regard to remaining claims 1, 4, 5/1, 5/4, 7, 8, 14, 15, 18, 19, 25 and 26, Appellants respectfully request the Honorable members of the Board of Patent Appeals and Interferences to reverse each of the outstanding rejections in connection with the present application and allow each of these claims. Throughout the prosecution of the present application, the Examiner has applied and the withdrawn several rejections, each time failing to find at least a crossbar including N ports, with the ports including N-1 output buffers, each corresponding to another of the N-1 ports. No such teaching or suggestion is present in any of the prior art documents provided by the Examiner taken either singly or in combination. Accordingly, reversal of all outstanding rejections is respectfully requested.

This Appeal Brief is being presented in triplicate.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,
HARNESS, DICKEY, & PIERCE, P.L.C.

Dated: 3-23-04

By: _____
Donald J. Daley, Reg. No. 34,313

Please address all correspondence to:

Marvell Semiconductor, Inc.
700 First Avenue, Mail Stop 509
Sunnyvale, CA 94089
Customer No. 23624
Tel. No. (408) 222-2500
Fax. No. (408) 752-9034

APPENDIX A -- THE CLAIMS

This is a complete and current listing of the claims, marked with status identifiers in parentheses. The following listing of claims will replace all prior versions and listings of claims in the application.

1. (Previously Presented) A data network comprising:

at least one crossbar, wherein each crossbar comprises N ports;

a plurality N of devices each associated with and connected to one port of one of said crossbars;

wherein each one port of one crossbar comprises:

an input buffer for receiving messages from the device connected to its port and for sending said messages to the N-1 other ports of said one crossbar;

a plurality N-1 of port output buffers, each corresponding to one of said N-1 other ports, wherein each of said plurality of N-1 of port output buffers receives said messages only from a corresponding input buffer corresponding to one of said N-1 other ports;

a plurality N-1 of fullness sensors, each associated with one port output buffer, for measuring the fullness state of its associated port output buffer;

shutoff means, connected to the fullness sensors associated with the port output buffers corresponding to said one port at said N-1 other ports, for, when said fullness state for one of said other ports is generally full, indicating to said device connected to said one port not to send data for the port which is now generally full.

2. (Previously Presented) A data network comprising:

at least one crossbar, wherein each crossbar comprises N ports;

a plurality N of devices each associated with and connected to one port of one of said crossbars;

wherein each one port of one crossbar comprises:

an input buffer for receiving messages from the device connected to its port and for sending said messages to the N-1 other ports of said one crossbar;

a plurality N-1 of port output buffers, each corresponding to one of said N-1 other ports, wherein each of said plurality of N-1 of port output buffers receives said messages only from a corresponding input buffer corresponding to one of said N-1 other ports;

a plurality N-1 of fullness sensors, each associated with one port output buffer, for measuring the fullness state of its associated port output buffer;

shutoff means, connected to the fullness sensors associated with the port output buffers corresponding to said one port at said N-1 other ports, for, when said fullness state for one of said other ports is generally full, indicating to said device connected to said one port not to send data for the port which is now generally full,

wherein each device additionally comprises N-1 device output buffers, one per the N-1 other ports of said crossbar.

3. (Original) A network according to claim 2 and wherein each device also comprises a multiplicity of direct memory access (DMA) units for removing data from at least one of said device output buffers.

4. (Original) A network according to claim 1 and wherein each crossbar comprises an arbiter for providing said messages from said N-1 port output buffers to said device connected to its port only if said device is not full.

5. (Previously Presented) A network according to any of the preceding claims 1-4, and wherein each port comprises a bus link connected to said corresponding associated device.

6. (Cancelled)

7. (Previously Presented) A crossbar for communicating with at least one device, said crossbar comprising:

N ports, each one of said N ports comprising:

a link logic unit to receive messages and data from a respective device,

an input buffer to store data from the respective device,

N-1 output buffers each corresponding to another one of said N-1 ports; and

a port arbiter to select one of said N-1 output buffers to output data to the respective device,

wherein said input buffer transfers the stored data to the corresponding output buffer of a selected one of the other one of said N ports.

8. (Previously Presented) A crossbar according to Claim 7, wherein said link logic unit determines a type of message from the respective device.

9. (Previously Presented) A crossbar according to Claim 8, wherein if the type of message is a local link message, a port function is performed and the message is not transferred.

10. (Previously Presented) A crossbar according to Claim 8, wherein if the type of message is a switch link message, the message and the data are transferred.

11. (Previously Presented) A crossbar according to Claim 7, wherein said device comprises one of a switch and a second crossbar.

12. (Previously Presented) A crossbar according to Claim 11, wherein said N-1 output buffers comprises a device table register to store a device number if the device comprises the switch.

13. (Previously Presented) A crossbar according to Claim 11, wherein said N-1 output buffers comprises a device table register to store device numbers of devices connected to the second crossbar.

14. (Previously Presented) A crossbar according to Claim 7,

wherein if the device is unable to receive data, the device provides a message to said link logic unit, and

wherein said link logic unit signals said arbiter to inhibit communication to the device.

15. (Previously Presented) A crossbar according to Claim 7,

wherein if an n^{th} one of said of said N-1 output buffers is at least a predetermined capacity, a signal is sent to the n^{th} one of said port arbiter of the other one of said N-1 ports to inhibit further transmission.

16. (Previously Presented) A network switch in communication with one port of a crossbar having N ports, said network switch comprising:

N-1 output buffers, each corresponding to N-1 other ports of the N ports of the crossbar, each of said N-1 output buffers comprising:

a direct memory access unit, and

a FIFO; and

an arbiter for controlling communications between said N-1 output buffers and the crossbar,

wherein when the crossbar signals said arbiter to inhibit sending data to an n^{th} one of the N-1 other ports, an n^{th} direct memory access unit stops transferring data from an n^{th} FIFO while other ones of said N-1 direct memory access units are not inhibited from transferring data.

17. (Previously Presented) A network apparatus comprising:

a crossbar for communicating with at least one device, said crossbar comprising:

N ports, each one of said N ports comprising:

a link logic unit to receive messages and data from a respective device,

an input buffer to store data from the respective device,

N-1 output buffers each corresponding to another one of said N-1 ports; and

a port arbiter to select one of said N-1 output buffers to output data to the respective device,

wherein said input buffer transfers the stored data to the corresponding output buffer of a selected one of the other one of said N ports,

wherein said at least one device comprises:

a network switch in communication with an m^{th} port of said crossbar, said network switch comprising:

N-1 output buffers, each corresponding to N-1 other ports of the N ports of said crossbar, each of said N-1 output buffers comprising:

a direct memory access unit, and

a FIFO; and

an arbiter in communication with said port arbitor for controlling communications between said N-1 output buffers and the crossbar,

22. (Previously Presented) A crossbar according to Claim 18, wherein said device comprises one of a switch and a second crossbar.

23. (Previously Presented) A crossbar according to Claim 22, wherein said N-1 output buffer means comprises a device table register means for storing a device number if the device comprises the switch.

24. (Previously Presented) A crossbar according to Claim 22, wherein said N-1 output buffer means comprises a device table register means for storing device numbers of devices connected to the second crossbar.

25. (Previously Presented) A crossbar according to Claim 18,

wherein if the device is unable to receive data, the device provides a message to said link logic means, and

wherein said link logic means signals said arbiter means to inhibit communication to the device.

26. (Previously Presented) A crossbar according to Claim 18,

wherein if an n^{th} one of said of said N-1 output buffer means is at least a predetermined capacity, a signal is sent to the n^{th} one of said port arbiter means of the other one of said N-1 port means to inhibit further transmission.

27. (Previously Presented) A network switch in communication with one port of a crossbar having N port means, said network switch comprising:

N-1 output buffer means, each corresponding to N-1 other port means of the N port means of the crossbar, each of said N-1 output buffer means comprising:

direct memory access means for controlling memory access, and

FIFO buffer means for storing data; and

arbiter means for controlling communications between said N-1 output buffer means and the crossbar,

wherein when the crossbar signals said arbiter means to inhibit sending data to an n^{th} one of the N-1 other port means, an n^{th} direct memory access means stops transferring data from an n^{th} FIFO buffer means while other ones of said N-1 direct memory access means are not inhibited from transferring data.

28. (Previously Presented) A network apparatus comprising:

crossbar means for communicating with at least one device, said crossbar means comprising:

N port means, each one of said N port means comprising:

link logic means for receiving messages and data from a respective device,

input buffer means for storing data from the respective device,

N-1 output buffer means each corresponding to another one of said N-1 port means; and

port arbiter means for selecting one of said N-1 output buffer means to output data to the respective device,

wherein said input buffer means transfers the stored data to the corresponding output buffer means of a selected one of the other one of said N port means,

wherein said at least one device comprises:

network switch means for communicating with an m^{th} port of said crossbar, said network switch means comprising:

N-1 output buffer means, each corresponding to N-1 other port means of the N port means of said crossbar means, each of said N-1 output buffer means comprising:

direct memory access means, and

FIFO buffer means; and

arbiter means in communication with said port arbitor for controlling communications between said N-1 output buffer means and the crossbar,

wherein when said crossbar signals said arbiter means to inhibit sending data to an n^{th} one of said N-1 other port means, an n^{th} direct memory access means stops transferring data from an n^{th} FIFO BUFFER MEANS while other ones of said N-1 direct memory access means are not inhibited from transferring data.

US 093488650JP1

Creation date: 09-28-2004
Indexing Officer: TBUI1 - THU-TRANG BUI
Team: OIPEBackFileIndexing
Dossier: 09348865

Legal Date: 05-18-2004

No.	Doccode	Number of pages
1	SRNT	10

Total number of pages: 10

Remarks:

Order of re-scan issued on .....